Library Characterization and Static Timing Analysis of Single-Track Circuits in GasP

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Acknowledgements

Thesis Committee

- Dr. Xiaoyu Song (chair) (ECE)
- Dr. Douglas V. Hall (ECE)
- Dr. Christof Teuscher (ECE)
- Marly Roncken (CS, ARC)

Special Thanks

- Ivan Sutherland (ECE, ARC)

Introduction: GasP

Fast Asynchronous Symmetric Pulse Protocol

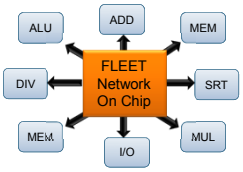
- Uses Single-Track Handshake signaling
- Light-weight in area and in power
- Flexible elastic communication

Flexibility + High Speed + Low Power + Low Area

- Makes an excellent circuit family for on-chip communication

More details on:

- http://arc.cecs.pdx.edu

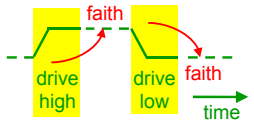


Important for Multi-core and Parallel systems

Introduction (2): Single-Track Handshaking

- Bi-directional 1-wire communication
- Request=high, Acknowledge=low
- 2-phase return-to-zero handshake

- Wire is driven briefly
- $Wire_{end1}$ starts/stops up-transition
- $Wire_{end2}$ starts/stops down-transition



requires FAITH in engineering and tools

ASSUMPTION-1:

- The brief drive is long enough to get the transition to the other end

ASSUMPTION-2:

- Voltage observed at the near-end reflects the voltage at the far-end

Introduction (3): Putting Things in Perspective

FAITH versus MEASUREMENT

- In GasP we use FAITH where we CAN
- and MEASUREMENT where we MUST

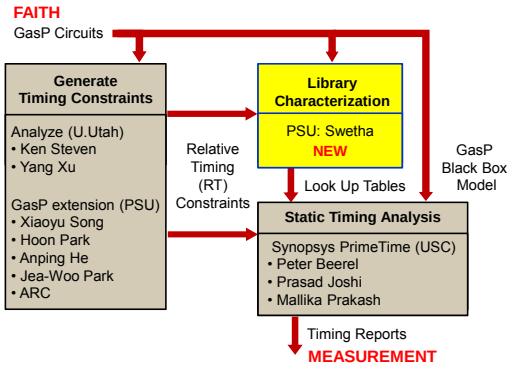
Thesis Goal:

- Develop a timing validation flow
- that translates FAITH into MEASUREMENT

Scope:

- GasP is the study target
- but the results apply also to other single-track families

Introduction (4): Timing Validation Flow



Outline

- GasP and its Relative Timing Constraints
- Library Characterization
  - Partition Relative Timing Constraints
  - Generate Simulation Environment
  - Generate Look Up Tables
- Static Timing Analysis
  - Run USC flow with my Look Up Tables
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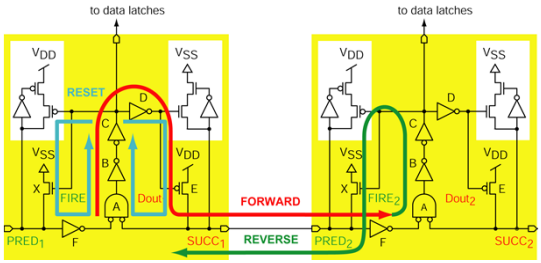
- Conclusion and Future Work

6-4 GasP

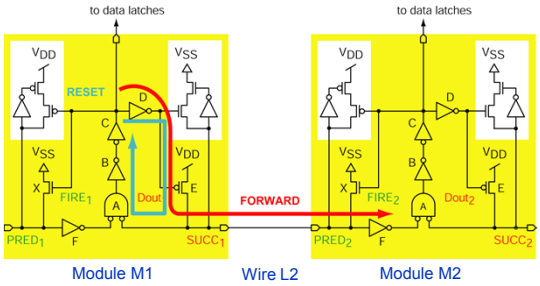
Cycle time: 6 gates FORWARD + 4 gates REVERSE = 10



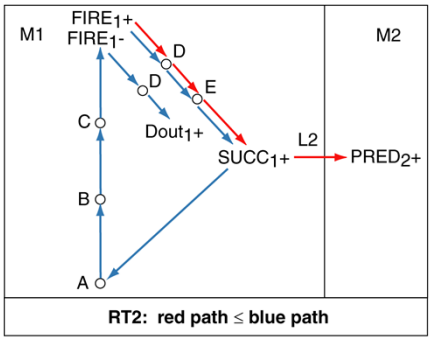
6-4 GasP

Relative Timing Constraint RT2:

FORWARD delay ≤ RESET delay



Another Way to Represent Constraint RT2



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Outline - Reminder

- GasP and its Relative Timing Constraints
- Library Characterization
  - Partition Relative Timing Constraints
    - Cut RT paths into smaller paths that are easy to characterize
    - i.e. easy to simulate for various input slopes and output loads
    - Solution: cut at the inputs and outputs of the circuit
- Static Timing Analysis
  - Run USC flow with my Look Up Tables
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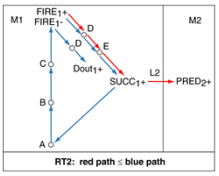
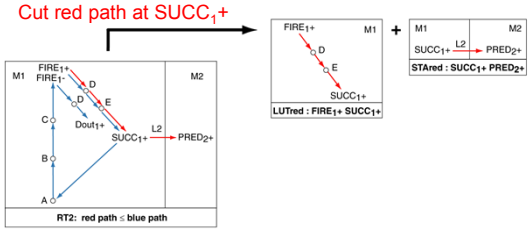
Partition RT2 constraint



Partition RT2 constraint

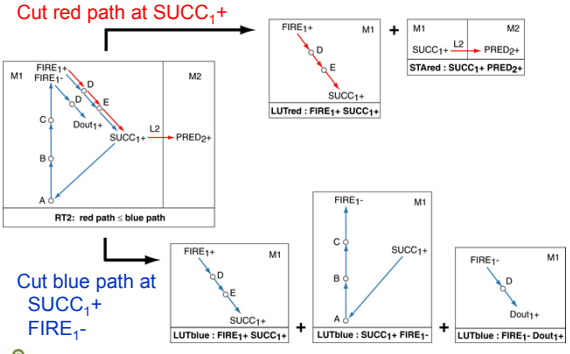
Cut red path at $SUCC_1+$



Partition RT2 constraint

Cut red path at $SUCC_1+$

Cut blue path at $SUCC_1+$ $FIRE_1-$



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Outline - Reminder

- GasP and its Relative Timing Constraints
- Library Characterization
  - Partition Relative Timing Constraints
  - Generate Simulation Environment
    - Cut the circuit into smaller sub-circuits that fit the sub-paths
    - Add circuitry to simulate min-max delays and reset single-track wires
    - Embed in a final setup for sweeping input slopes and output loads
- Static Timing Analysis
  - Run USC flow with my Look Up Tables
  - Inspect Timing Reports
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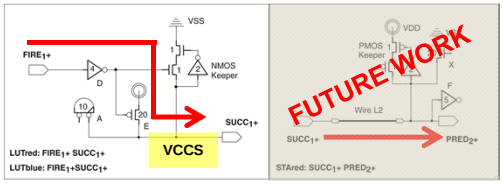
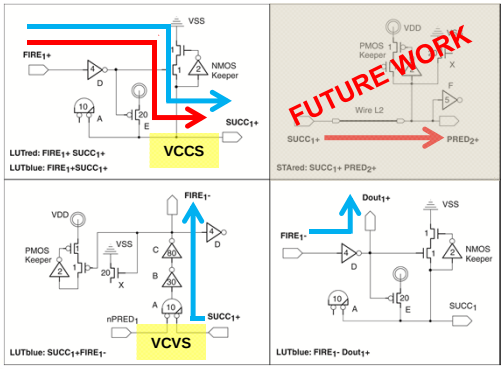
Partition the 6-4 GasP circuit for RT2



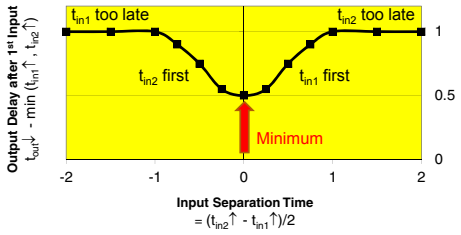
Partition the 6-4 GasP circuit for RT2



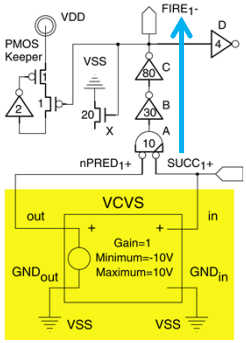
First Circuit Enhancement for RT2

What:

- Minimize the (BLUE) Reset Loop Delay
- by minimizing the delay of NOR-function A going down



First Circuit Enhancement for RT2 - continued



How:

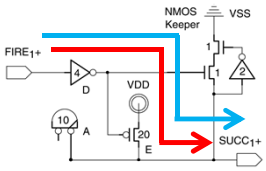
by using a "demon in a box"
Voltage Controlled Voltage Source

- That copies V(SUCC$_1$) to V(nPRED$_1$) without extra delay or load

The VCVS in this picture

- Minimizes the falling delay of gate A
- and thus the delay of RT2 sub-path LUTblue:SUCC$_1$+FIRE$_1$-

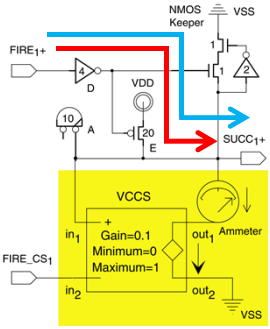
Second Circuit Enhancement for RT2



What:

- Module M1 can only raise SUCC$_1$ because it's a single-track signal
- So: SUCC$_1$ must be re-initialized before the next simulation cycle

Second Circuit Enhancement for RT2



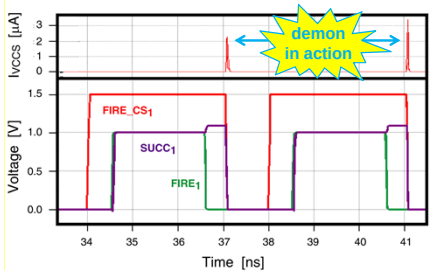
What:

- Module M1 can only raise SUCC$_1$ because it's a single-track signal
- So: SUCC$_1$ must be re-initialized before the next simulation cycle

How: another "demon in a box"
Voltage Controlled Current Source

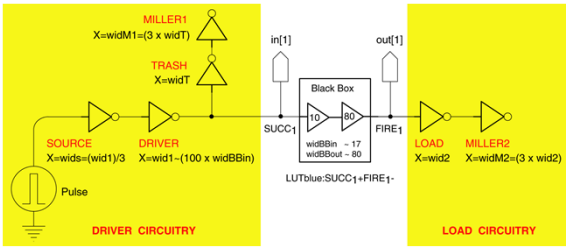
- That uses as completion pulse signal FIRE_CS$_1$ to reset SUCC$_1$
- by translating the surplus voltage on SUCC1 into a drain current
- without delaying or loading SUCC$_1$+

Relationship FIRE_CS$_1$ to FIRE$_1$ and SUCC$_1$



- Reset: SUCC$_1$ falls after FIRE$_1$ falls and before FIRE$_1$ rises
- Measurement: SUCC$_1$ rises within the FIRE$_1$ high-pulse window
- Mutual exclusion: VCCS drain current = 0A during the FIRE$_1$ high-pulse

Final Simulation Setup



- Sweep: Trash size widT (driver circuitry) and Load size wid2 (load circuitry)
- Measure: Timing and Voltage changes on in[1] and out[1]
- Result: (widT x wid2) → slope(in[1]) , delay(in[1] to out[1]), slope(out[1])

… and the Look Up Table that it generates

LUTblue:SUCC1+FIRE1-

Output Load [fF] \ Input Slope [ps]	14.2		15.1		16.3		21.4	
	delay [ps]	output slope [ps]	delay [ps]	output slope [ps]	delay [ps]	output slope [ps]	delay [ps]	output slope [ps]
0.0	35.8	8.8	36.3	8.6	37.4	8.5	39.2	8.3
18.2	37.7	10.0	38.0	10.1	39.3	9.6	40.8	10.8
59.3	41.6	13.8	41.9	14.2	43.0	13.9	44.7	13.9
101.4	45.0	18.0	45.3	18.0	46.3	18.3	48.1	18.2
142.8	48.0	22.8	48.4	22.5	49.3	22.8	51.2	22.7
185.1	50.9	26.9	51.2	27.0	52.1	27.1	54.0	27.0

- Stores: (Input Slope x Output Load) → delay(in[1] to out[1]), slope(out[1])

… is used as follows

LUTblue:SUCC1+FIRE1-

Output Load [fF] \ Input Slope [ps]	14.2		15.1		16.3		21.4	
	delay [ps]	output slope [ps]	delay [ps]	output slope [ps]	delay [ps]	output slope [ps]	delay [ps]	output slope [ps]
0.0	35.8	8.8	36.3	8.6	37.4	8.5	39.2	8.3
18.2	37.7	10.0	38.0	10.1	39.3	9.6	40.8	10.8
59.3	41.6	13.8	41.9	14.2	43.0	13.9	44.7	13.9
101.4	45.0	18.0	45.3	18.0	46.3	18.3	48.1	18.2
142.8	48.0	22.8	48.4	22.5	49.3	22.8	51.2	22.7
185.1	50.9	26.9	51.2	27.0	52.1	27.1	54.0	27.0

delay(12.24ps ,0fF)= ?

slope(12.24ps, 0fF)= ?

… is used as follows

LUTblue:SUCC1+FIRE1-

Output Load [fF] \ Input Slope [ps]	14.2		15.1		16.3		21.4	
	delay [ps]	output slope [ps]	delay [ps]	output slope [ps]	delay [ps]	output slope [ps]	delay [ps]	output slope [ps]
0.0	35.8	8.8	36.3	8.6	37.4	8.5	39.2	8.3
18.2	37.7	10.0	38.0	10.1	39.3	9.6	40.8	10.8
59.3	41.6	13.8	41.9	14.2	43.0	13.9	44.7	13.9
101.4	45.0	18.0	45.3	18.0	46.3	18.3	48.1	18.2
142.8	48.0	22.8	48.4	22.5	49.3	22.8	51.2	22.7
185.1	50.9	26.9	51.2	27.0	52.1	27.1	54.0	27.0

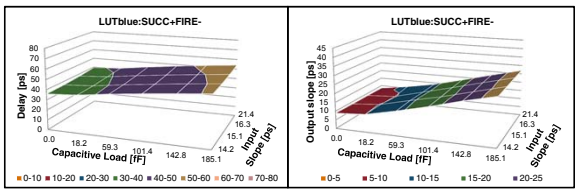
delay(12.24ps ,0fF)= 35.8 –(((14.2 – 12.24) / (15.1 – 14.2)) x (36.3 – 35.8)) = 34.71 ps

slope(12.24ps, 0fF)= 8.8 –(((14.2 – 12.24) / (15.1 – 14.2)) x (8.6 – 8.8)) = 9.24 ps

Landscape Graphs for the Look Up Table

DELAY landscape
(color distinction every 10 ps)

OUTPUT SLOPE landscape
(color distinction every 5 ps)



BOTH are very amenable to linear approximation techniques

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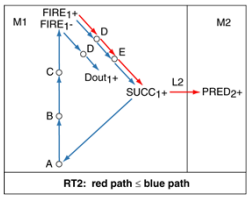
Timing Report for RT2

```
*************************************
Report : timing
       -path_type full
       -delay_type max
       -max_paths 1
Design : GASP_FIFO2
Version: C-2009.06-SP3
Date   : Mon Oct 11 10:28:45 2010
*************************************

  Startpoint: M1/FIRE (clock source 'M1/FIRE')
  Endpoint: M2 (rising edge-triggered data to data check
                                        clocked by M1/FIRE)
  Path Group: M1/FIRE
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------
  clock M1/FIRE (rise edge)                0.00       0.00
  clock source latency                     0.00       0.00
  M1/FIRE (GASP_Module)                    0.00       0.00 r
  M1/SUCC_OUT (GASP_Module)               26.36      26.36 f
  M2/PRED_IN (GASP_Module)                 0.00      26.36 f
  data arrival time                                  26.36

  clock M1/FIRE (rise edge)                0.00       0.00
  clock source latency                     0.00       0.00
  M1/FIRE (GASP_Module)                    0.00       0.00 r
  M1/SUCC_OUT (GASP_Module)               26.36      26.36 r
  M1/FIRE_DS (GASP_Module)                34.71      61.07 r
  M1/Dout (GASP_Module)                   19.32      80.39 r
  data check setup time                    0.00      80.39
  data required time                                 80.39
  ---------------------------------------------------------
  data required time                                 80.39
  data arrival time                                 -26.36
  ---------------------------------------------------------
  slack (MET)                                        54.03
```



RED path delay = 26.36 ps

BLUE path delay = 80.39 ps

RT2 is satisfied
Slack = 54.03 ps

Conclusion and Future Work

Take-Away:

- We now have a Timing Validation flow for single-track circuits
  - It translates FAITH (design assumptions) into MEASUREMENT
  - by generating Look Up Tables
  - that go into the USC Static Timing Analysis flow
  - which reports how well the FAITH holds up
- The proof of the pudding is in the eating
  - I used this flow to validate relative timing assumptions in 6-4 GasP
  - The results match with the results of my ASYNC 2010 publication

Future Work:

- Wire delay model
  - with near-end capacitive load and far-end delay information
- Flow automation