Verifying Timing Constraints for Delay-Insensitive Circuits

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Why does anyone verify timing in self-timed circuits? The fundamental reason is that only a limited class of circuits is truly insensitive to delays in gates and wires. The circuit is delay-insensitive only if each handshake component faithfully follows the protocols.
By carefully considering time locally we can ignore time globally.

ARCtimer is a framework to identify internal timing constraints. Through ARCtimer, we have identified timing constraint patterns for the entire Click circuit family. This flow can handle data as well as non-deterministic internal choice.

The spiral in the figure shows the four main steps in ARCtimer. ARCtimer is used early in the design process to build a Design Library of verified components for use in any chip design.

References

[1] W. Mallon. Theories and Tools for the Design of Delay-Insensitive Communicating Processes, Ph.D. thesis, University of Groningen, 2000.
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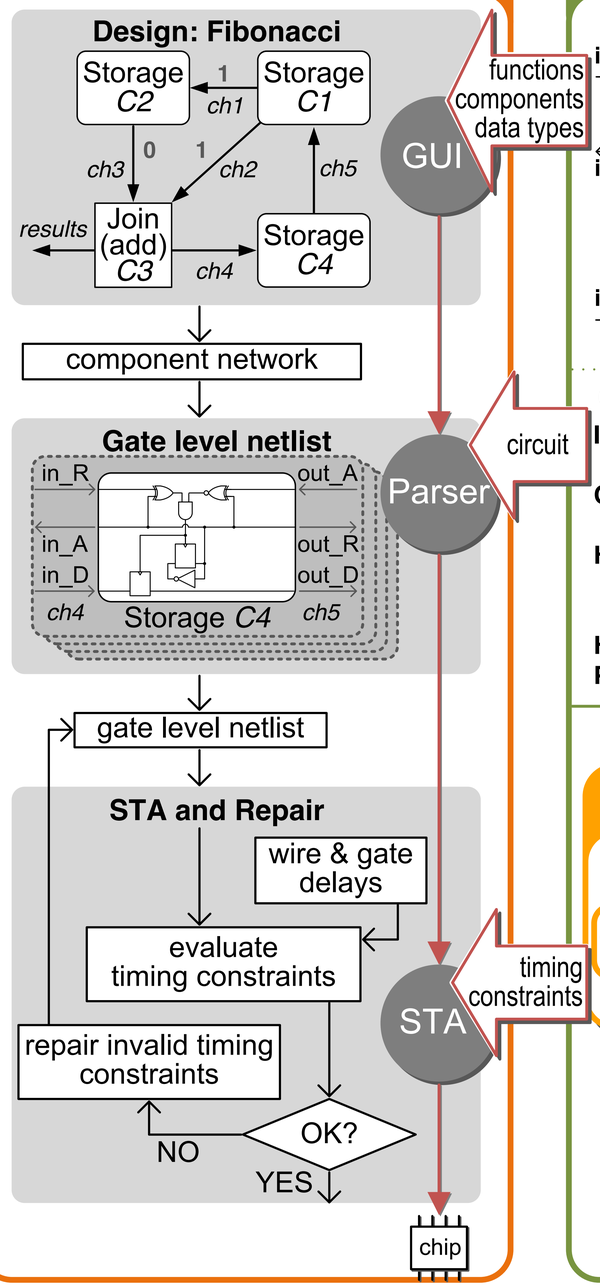
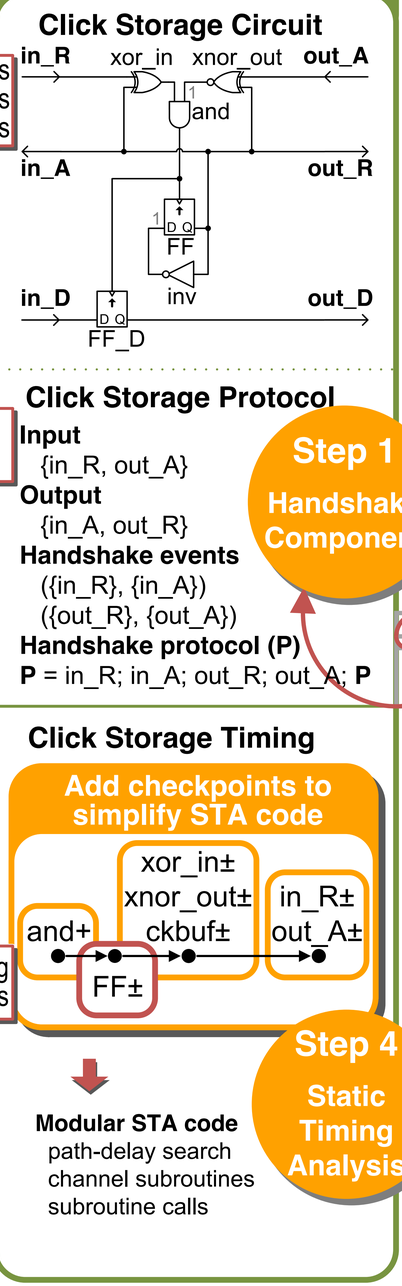
[3] H. Park, A. He, M. Roncken, X. Song. Semi-modular delay model revisited in context of relative timing, Electronics Letters (IET), Volume 51, Issue 4, pages 332-334, 2015.
[4] H. Park, A. He, M. Roncken, X. Song, I. Sutherland. Modular Timing Constraints for Delay-Insensitive Systems, *to appear in* Journal of Computer Science and Technology (JCST), 2015.

Chip Design



Design Library



Timing Pattern Generation & Verification