ASYNCHRONOUS RESEARCH CENTER

Portland State University

Subject: **Second Class Handout – GasP Rings**
Date: **October 1, 2010**
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ARC#: **2010-is44**

References:

ARC# 2010-is43: Class 1 – Ring Oscillators, Ivan Sutherland, 1 September 2010
Sutherland, I.E., "Micropipelines," Communications of the ACM, June 1989.
Sutherland, I.E., & Fairbanks, S., "GasP: A Minimal FIFO Control," Proceedings of the Seventh International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC 2001), April 2001
http://fleet.cs.berkeley.edu/docs/ and click on ies49 A Six Four GasP Tutorial

PURPOSE

This memo introduces the basic six-four GasP circuit. In class we will do a Kinetic Learning Activity to illustrate self-timed pipelines.

SIX-FOUR GasP

Consider Figures **gaspAempty** and **gaspAfull**, which you can also find on the ARC web site. These are "bare bones" six-four GasP circuits. These two circuits are the same except for an initial condition applied to the predecessor state wire. In this assignment you'll simulate a ring of such circuits to see how they work.

The Six-Four GasP Tutorial available on the Berkeley web site offers a lot of information about six-four GasP. Examine it if you wish, but it's got more detail than you need just now.

The circuits for this assignment have two simplifications. First, all of the logic gates have the same strength, X=10. Second, "keepers" are omitted; we'll learn about them later. The circuits "gaspAfull" and "gaspAempty" for this assignment place the logic gates in both circuits so that they all point up at equal vertical spacing. This regular geometric arrangement of logic gates helps us to understand timing.

Notice the two loops in these circuits; you should recognize them from our discussion last week; see notes ARC# 2010-is43. On the left of the figure you can see a loop whose state wire is called `pred`. On the right of the figure you can see a loop whose state wire is called `succ`. The two loops share three logic elements up the center of the figure.

Each of these two loops contains five logic gates; count them. Each loop is a ring oscillator of five inverters with two minor differences. The first difference is that one gate in each ring, the isolated N-type or P-type transistor at the top, is only half of an inverter. The other half of that inverter lies in an adjacent GasP module. The N-type transistor in the predecessor loop can drive the predecessor state wire to LO only, meaning empty. The P-type transistor in the successor loop can drive the successor state wire to HI only, meaning full.

The second difference is the AND function that joins the two loops. Its output can go HI only when both its inputs are LO. The output of the AND function goes HI only when both A) the predecessor is full, and B) the successor is empty. After amplification by two inverters in series, this action becomes the output signal called `fire`. Later on we will use `fire` to render some data latches associated with this GasP control stage momentarily transparent. For now we'll omit the data latches.

Each time `fire` goes HI, three things happen as an indivisible "atomic" operation. First, the `fire` pulse causes the latches, not shown, to copy data. Second, the predecessor state becomes LO, meaning empty. And third, the successor state wire becomes HI, meaning full.

Icons. Electric combines sub-circuits into a hierarchy. Each sub-circuit can have one or more icons. The icons for our two GasP circuits appear in the upper right of their schematics. Each icon you place in a higher-level circuit represents a separate instance of its circuit. You can go "down" into an icon to see the circuit it represents. Indeed, the red symbols for logic gate in these figures are themselves icons for the combinations of transistors that make up the logic gate. The inverter circuit has two different icons, one with bubble at the input and one with the bubble at the output. If you go down into either icon you'll see the very same inverter circuit.

Exports: Electric lets you "export" any connection from a sub-circuit so that you can connect to it at a higher level. Each of our two GasP circuits "exports" three connections: `pred`, `succ` and `fire`. The two red diamonds and the red arrow symbol identify the exports. The shape of the red export symbol shows the type of the export. The diamonds for `pred` and `succ` show that `pred` and `succ` are "bi-directonal." The arrow shape for `fire` shows that it is an output. These circuits don't have any pure inputs; if they did we'd see an arrow symbol facing in. You can see labels for the three export attachments in the icon symbols at the upper right of the figures.

A RING OF GasP

Let us connect ten icons for these GasP circuits into a ring. The figure called "ringOf10" actually has two such rings. Notice that the `succ` connection of each icon attaches to a `pred` connection on the next icon. The short horizontal wires between the icons in this figure are the state wires, sw[1:9]. Recall that the colon separating the first and last number indicates that we mean all indices in between. The long "loop back" wire above the icons, sw[10], is also a state wire. Altogether in the two rings there are 20 state wires, sw[1:20]. Each state wire links two GasP circuits, one of which can drive the state wire only HI, while the other GasP circuit can drive the state wire only LO.

Notice that in the upper ring all but one of the icons carry the notation "empty." In the lower ring, all but one of the icons carry the notation "full." The only distinction between our two GasP circuits is the initial condition set on their predecessor state wire. Thus when simulation starts, sw[1:9] will be LO and sw[10] will be HI.

QUESTIONS TO THINK ABOUT – turn in the answer sheet.

How long will the fire signal remain HI? How frequently can there be a fire pulse from one GasP circuit? In a ring of GasP modules, what is the relationship between the fire signal of one GasP module and that of its neighbors?

Why can we use an even number of GasP modules in a ring? Shouldn't the number be odd or maybe even prime. When I first simulated a ring of GasP modules I used an odd number, "just to be safe." How little I knew.

HOME ASSIGNMENT:

Simulate the two rings circuit. Do the rings oscillate? How long does it take for the action to pass around the ring? Divide the number of stages by that time to get the advance rate measured in stages per second. If the ring is nearly full, how long does it take for a "bubble" to pass backwards around the ring? What is the reverse rate in stages per second? Is the reverse rate larger or smaller than the advance rate?

We also refer to the forward latency. The forward latency is the time delay between when one stage fires and its successor stage fires. What is the forward latency for these circuits? What is the reverse latency? What does the name 6/4 GasP really mean?

The ambitious student will want to change these rings to have two full or two empty stages rather than only one. Hint: Electric offers a "change" function that lets you substitute one icon for another that has the same exports. You can very easily modify the rings to have different numbers of full and empty stages. What happens if you place two full stages with one or two empty stages between? Is such a pattern stable? Why?

ANSWER SHEET – due by beginning of class on 13 October 2010 **2**

Name _____ Turned in on Date _____

Answer by examining the circuits – no simulation required for these questions:

The fire signal will remain HI for approximately _____ gate delays.

Fire signals from a GasP circuit can happen no more often than every ____gate delays.

The soonest the next GasP module can fire is _____ gate delays after its predecessor.
Hint : count the gates.

The soonest the previous GasP module can fire is ____ gate delays after its successor.
Hint : count the gates.

Why can we use an even number of GasP modules in a ring?
Answer on the back of this paper if necessary.

Answer from simulation:

My simulation uses _____ technology – e.g. 180 MOSIS

It takes _____ nsec for a token to pass around the upper, mostly empty, ring.

It takes _____ nsec for a bubble to pass around the lower, mostly full, ring.

My simulation shows _____ psec/stage as the forward latency.

My simulation shows _____ psec/stage as the reverse latency.

Why is the reverse latency less than the forward latency?
Hint : count the gates. Answer on the back of this paper if necessary.

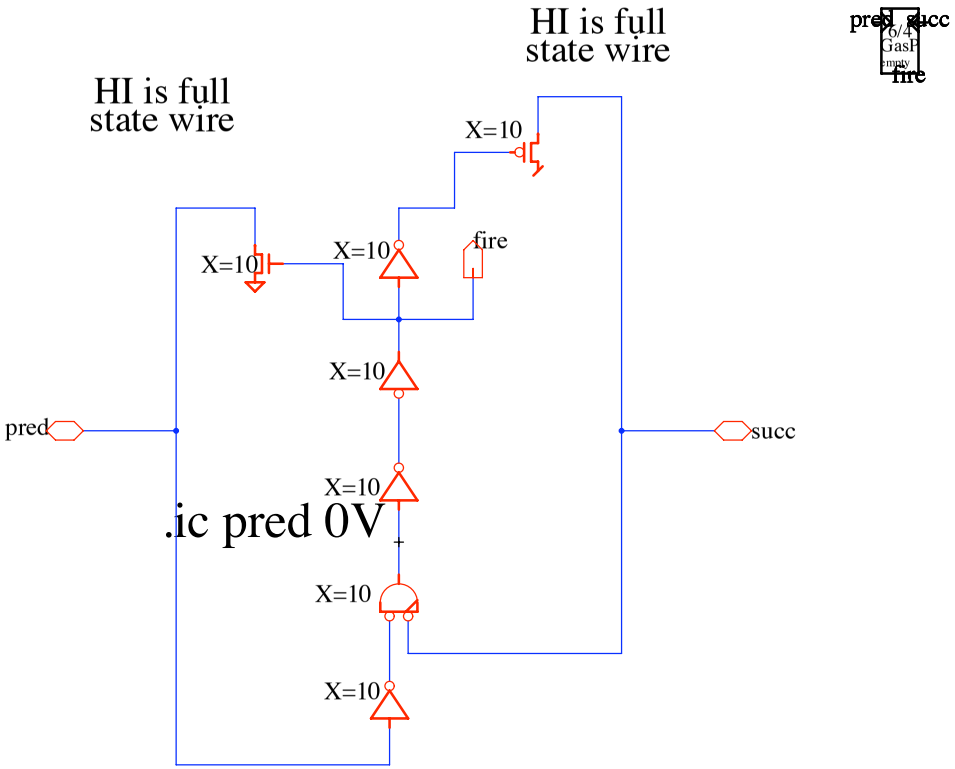
The number of inverting gates in a ring oscillator must be _____
but any two or more GasP modules can form a ring.

Optional: Start with two "full" stages. It takes _____nsec for both tokens to pass around the ring of ten stages.

Very Optional: Make a "canopy diagram" plotting throughput for zero to 10 full stages.

gaspAempty

nsk 2 September 2010



gaspAfull

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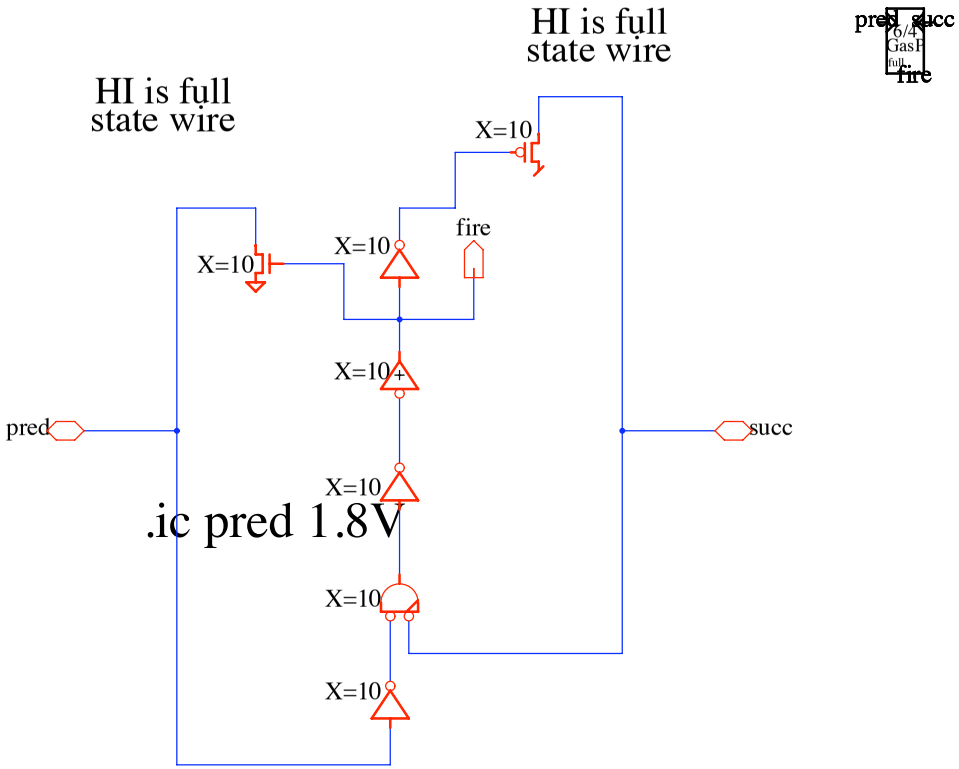

ringOf10

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