ASYNCHRONOUS RESEARCH CENTER

Portland State University

Subject: **The GasP Tutorial Aids**
Date: **August 25, 2009**
From: **Ivan Sutherland**
ARC#: **2009-is26**

References:

ARC# 2009-is25: Three Seven GasP, Ivan Sutherland, 18 August 2009

PURPOSE

This document carries figures intended to teach the GasP family of circuits.

THE FIGURES

This memo includes four figures in each of two sizes. Two of the figures are columns of logic with red labels at the top saying **NAND** and **NOR**. The other two are "state wires" labeled **HI is full** and **LO is full**. In the smaller size, all four of the figures fit on one page. The larger size NAND and NOR figures share a page, but each of the state wire figures appears on its own page.

You must cut the figures into vertical strips for them to fit together. You will need to cut up more than one copy of each figure to have enough parts. Cut each figure into a vertical strip with horizontal wires reaching all the way to the right and left edges. It's OK to remove a little of the horizontal wires; your strips may be of any width.

You assemble a GasP circuit by lining up alternating state wire and logic strips. Each state wire must lie between two columns of logic gates. Their wires should connect. Some alignments will leave extra wires and extra logic that you must either ignore or remove.

You must respect the sense of the wires when you align the strips. A wire with a bubble may connect only to other wires with bubbles. *It is improper to connect a wire with a bubble to one that lacks a bubble.* There are only two valid alignments between a logic strip and a state wire strip. There should be very pale colored bands near the top of the strips help guide proper assembly, but these bands fail to reproduce on my black and white copier.

WHY THESE ARE VALID GasP CIRCUITS

I have carefully arranged the vertical spacing of the parts to make the figures fit together into valid GasP circuits. All of the logic gates are exactly the same height and the two connections on the state wire span exactly four logic gates. Thus, together with the N or P transistors at the top of the state wire, any valid assembly of a state wire and a logic gate column makes a five-inverter loop.

We choose the transistor widths in GasP circuits so that all logic gates have the same delay. Thus you may think of time as running uniformly upward in each of the columns of inverters. Each state wire participates in two five-inverter loops, each of which has a single transistor at the top. The transistor with the bubble is a P-type transistor that drives the state wire HI; the transistor without the bubble is an N-type transistor that drives the state wire LO. Because the other four logic gates in each loop have the same delay, one of the transistors turns off just when the other turns on, so they never "fight."

To make the delay in each logic gate the same, the gates increase in transistor width as one passes up the logic column. The topmost gate may be quite large because it may drive the load of many latches. The individual transistors that drive the state wire may also be large when there is a big load on the state wire. However, the gates near the bottom of the column of logic tend to be small.

ODD AND EVEN DELAYS

Let us first assemble the "HI is full six-four GasP" circuit most commonly illustrated. To do this, alternate several **NOR** columns with several **HI is full** state wires. It is best to use at least three logic columns and at least two state wires. Align each state wire as high as possible on the NOR column to its left and its right. You must shift the NOR columns vertically; each NOR column will be higher than the one to its left.

Now count the number of logic gates from one state wire to the next, including the isolated transistor. There are six in the forward direction but only four in the reverse direction. Because of the vertical spacing of the wires on the state wire strips, the sum of the forward and reverse delays will always be ten. If the forward delay is even, so will be the reverse delay.

GasP circuits whose forward and reverse delays are even use identical state wire types. If you want an odd forward or reverse delay you must use different state wire types. Try assembling a five-five GasP circuit using one **HI is full** and one **LO is full** state wire.

NAND vs. NOR

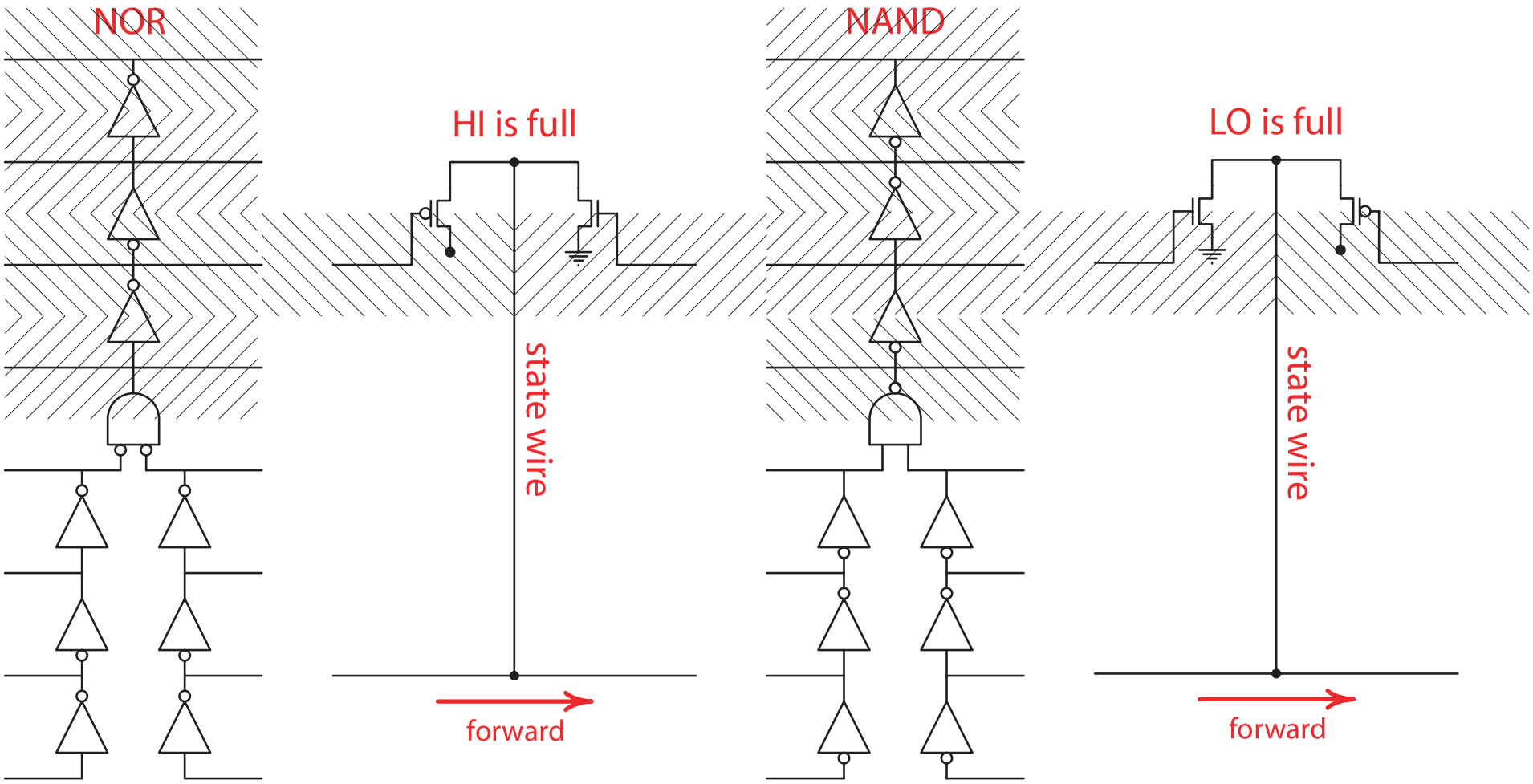
GasP circuits need an “AND” function to detect when the predecessor state wire is “full” and the successor state wire is “empty.” Both the NAND and the NOR logic columns provide such an AND function, in spite of the fact that they use slightly different logic types. De Morgan’s theorem lets you replace any NAND logic column with a NOR logic column displaced by one position. Try it.

The AND function in each logic column has inverters both before and after it. This also lets you displace the logic column up or down two positions with no change in logic function. Because the NAND or NOR gate requires more area than a simple inverter, I like to place my NAND or NOR function as near the bottom of the state wire connection as possible. By replacing the NAND with NOR or vice versa, it is always possible to make the output of one state wire or the other connect directly to it.

ONE-NINE GasP

With the parts provided here you can make almost any GasP circuit. You can have any forward delay from two to eight, and any reverse delay from eight to two, though their sum must be ten. One-nine and nine-one GasP are also possible, but I’ve avoided provide the necessary parts here.

One-nine and nine-one GasP require driving the state wire with two transistors in series. It is otherwise impossible to put the AND function near enough to the state wire to provide the single gate delay in the forward or reverse direction. I doubt that one-nine or nine-one GasP are useful.



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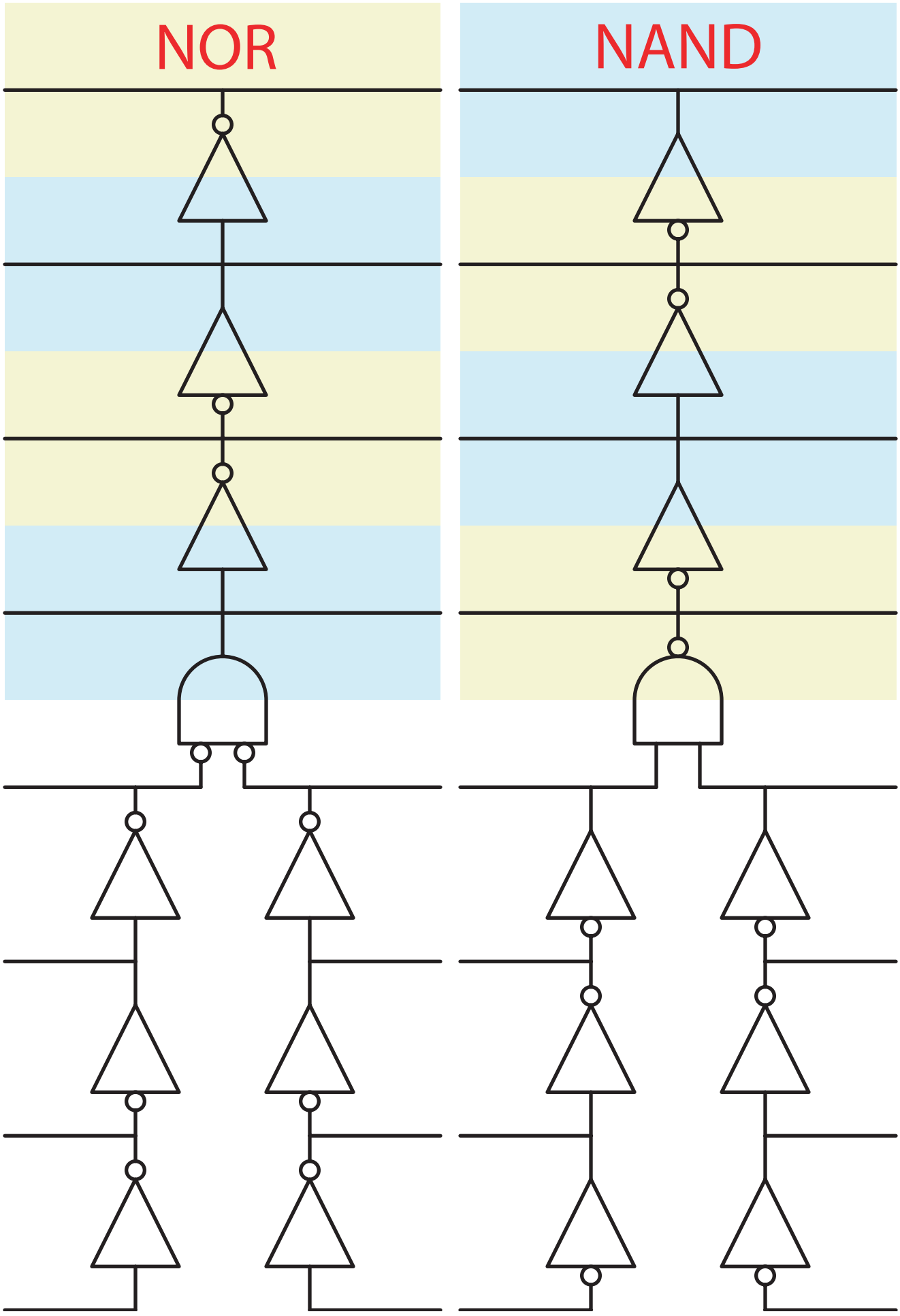
22 October 2009

Assemble GasP circuits


NOR
NAND

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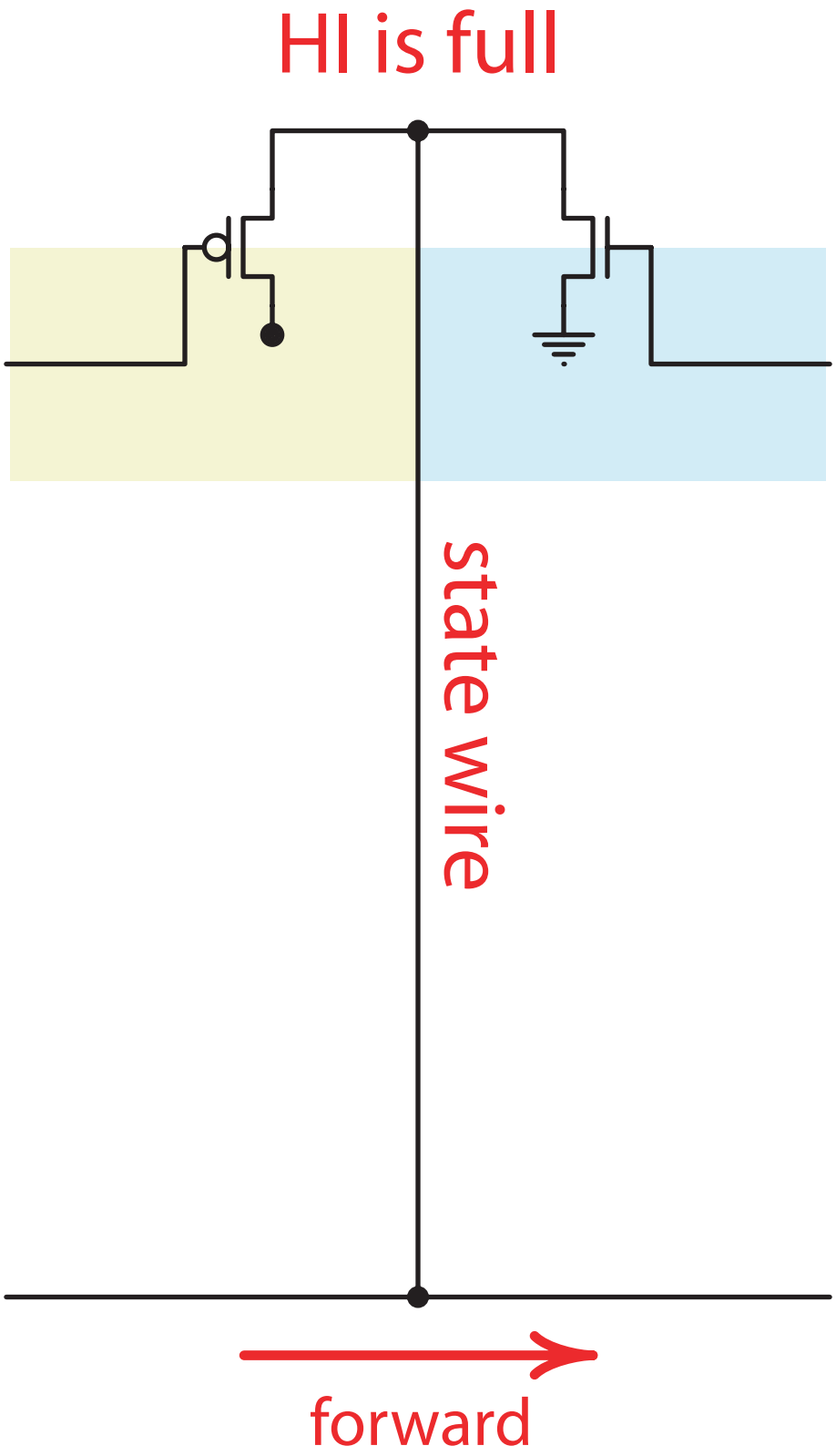

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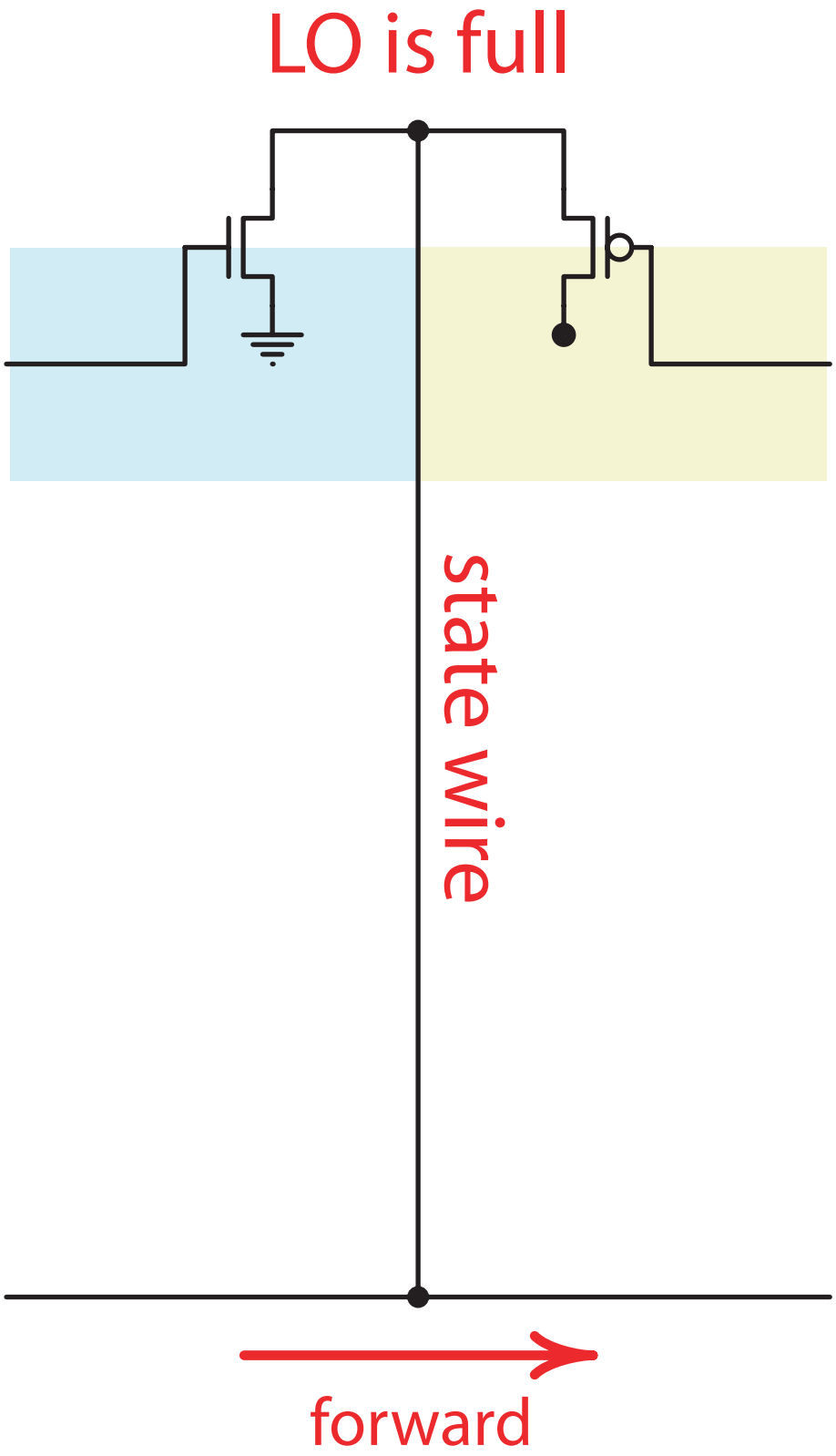

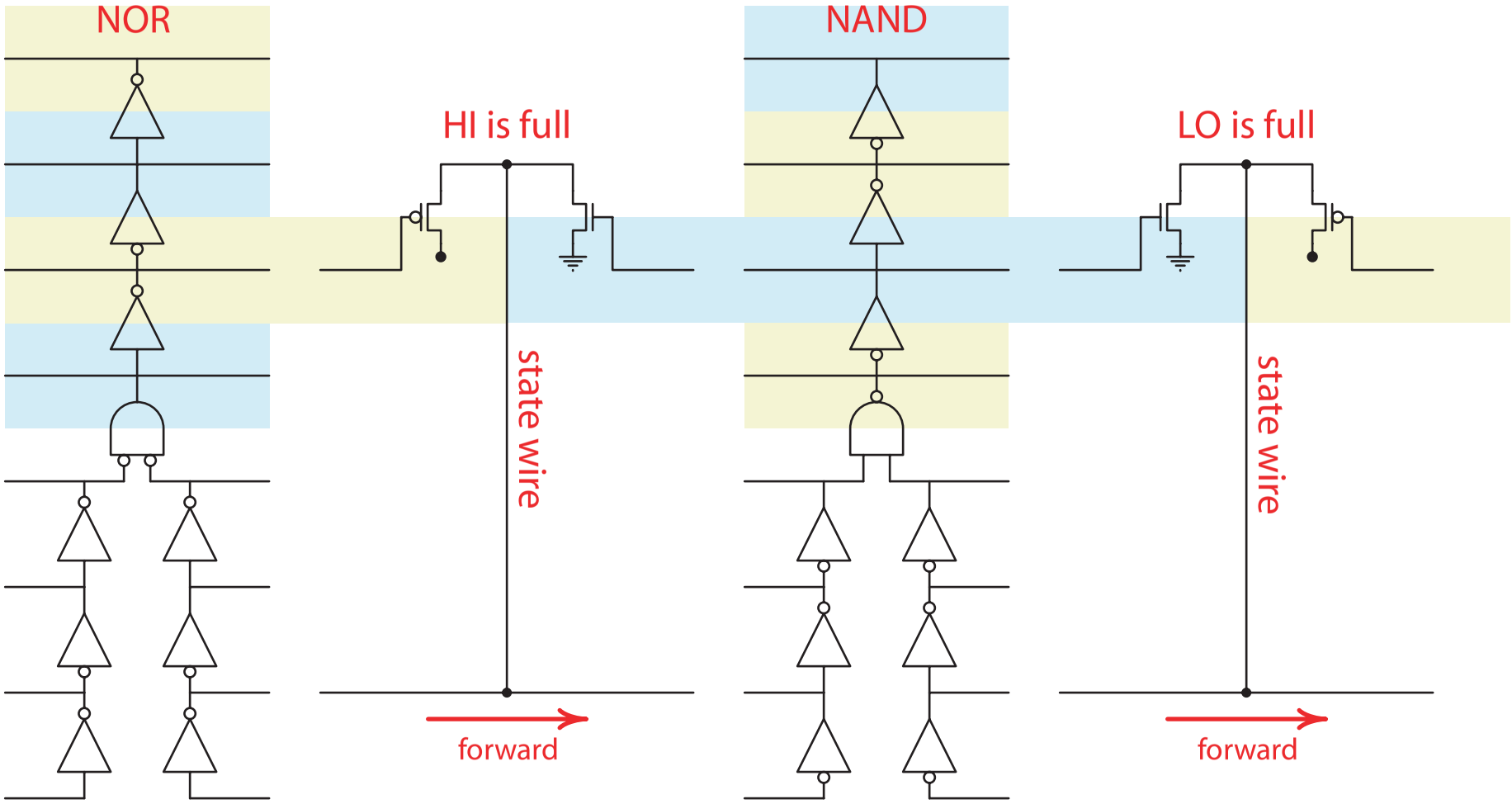

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