[Invited] State Access for RSFQ Test and Analysis

View Session Detail

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Abstract: We have developed means to initialize, read, maintain, change, and restore states in an RSFQ circuit that are useful for design as well as for test and analysis. Our test approach differentiates states by the information they carry from computation to computation and saves costs by ignoring information-free states.

States are abundant in RSFQ circuits, much more so than in a typical CMOS circuit. But as in CMOS, not all states are equal. We distinguish "enduring states," that carry information between computations, from "ephemeral states" that may change temporarily during a computation but remain the same before and after. We avoid test access to ephemeral states.

Enduring states play a key role in system initialization, test, and analysis. Crucially: the system behaves the same before and after "reading, destroying, and restoring" enduring states. Examples of enduring state holders in RSFQ are D2-latches and Non-Destructive-Read-Out (NDRO) latches; they store data inputs or computational results.

A key difference between an NDRO-latch and D2-latch is that the NDRO state outlives the read operation. To destroy the state of an NDRO-latch, one must explicitly reset the latch. Another key feature of an NDRO-latch is that the NDRO state remains in situ. This rarely mentioned feature is absent from for instance a RENDEZVOUS element, whose state vanishes to move along with the output, creating a moving target for test. Explicit reset and state immobility make NDRO-latches ideal building blocks for flow control, including repetition and asynchronous communication protocols, and for observability and controllability during test.

Based on these observations, we have developed a new variety of state holder that combines NDRO with RENDEZVOUS and D2-latch elements, and that provides the

flow control necessary to:
1. reliably start, stop, and restart operations,
2. stall operations until progress conditions are met, and
3. un-stall operations for re-initialization purposes.

These three capabilities are reflective of the “MrGO” circuit that facilitates initialization and test of asynchronous circuits in CMOS [Roncken:2015]. Our RSFQ test approach provides MrGO-like test and analysis for RSFQ circuits and can be enhanced with an IEEE 1149.1 test controller and scan chains. We have JoSIM supported simulation results showing functionality and throughput of clocked and asynchronous RSFQ designs with test access to enduring states only. We await layout resources to get chip-based experimental results.

[Roncken:2015] M. Roncken et al., “Naturalized Communication and Testing,” IEEE International Symposium on Asynchronous Circuits and Systems, 2015.