An IEEE-compatible JTAG Test-Access-Port Controller for RSFQ Logic and Systems

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Ivan Sutherland[*2,3], *Quinn Morgan*[1], *Warren Hunt*[4,3], *Vivek Ramanathan*[4,3], *Marly Roncken*[1]
[1]Computer Science Department, Portland State University, Portland, Oregon, United States; [2]Portland State University, Portland, Oregon, United States; [3]ForrestHunt, Inc, Austin, Texas, United States; [4]Computer Science, The University of Texas at Austin College of Natural Sciences, Austin, Texas, United States

Abstract: Even a perfect chip design may suffer manufacturing defects. Commercial chips undergo many tests: while on the wafer, after dicing, after packaging, and even after installation on a printed-circuit board. The IEEE JTAG/IEEE P1149.1 standard Test Access Port (TAP) Controller is widely included on commercial CMOS chips to facilitate such testing.
We have developed an RSFQ version of the IEEE standard TAP controller to facilitate testing superconducting circuits. The five-wire IEEE standard interface not only saves pins but also, in the cold environment, reduces heat loss. An eco-system of devices, knowledge, and instructional material has evolved around the IEEE standard TAP controller. We intend to make that eco-system useful to the superconducting community.
The IEEE standard tap controller is a 16-state, finite state machine that can send information to and receive information from any number of on-chip serial scan chains. Each scan chain is a serial-to-parallel and parallel-to-serial converter orchestrated by the TAP controller.
Nearly all complex RSFQ chips already use serial-parallel conversion to compress their input/output footprint. Scan chains are easy to assemble from a string of D2-Latches, each with two inputs and two outputs. Our TAP controller drives one side of the D2-Latches to pass data in parallel to or from a user's circuits. The other side of each D2-Latch shifts data serially along the scan chain to or from the TAP controller which, in turn, relays the data on or off chip.

The IEEE standard specifies the state transitions of our TAP controller. Our TAP control uses 16 D2-Latches in a one-hot-out-of-16 design. Each state advance passes the one-hot state from a sending state latch to a receiving state latch. The connections in or out of the TAP controller match exactly the state transitions of the IEEE standard. When in certain states, SHIFT, CAPTURE or UPDATE, our TAP controller delivers pulses to the user's scan chain to shift, capture, or update the scan chain's state. The IEEE standard reset sequence puts our TAP controller in its RESET state.
Our TAP controller occupies a space 550 microns wide and 70 microns high in the MIT-LL SFQ5EE process. It requires only five external signal pins in addition to separate latch and JTL bias pins. We expect to test it as part of a fabrication run planned for May 2022. The GDS and results of testing will be made publicly available.
We believe adoption of the IEEE test standard interface will facilitate testing superconductive logic chips, and it will make possible the remote testing of experimental superconducting chips. In fact, a single TAP controller could be used to test all devices on a multi-project chip. Widespread use of the IEEE standard test interface could make routine the remote testing of superconductive chips.

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