An IEEE-compatible JTAG Test-Access-Port Controller for RSFQ Logic and Systems

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Joint Test Action Group (JTAG)

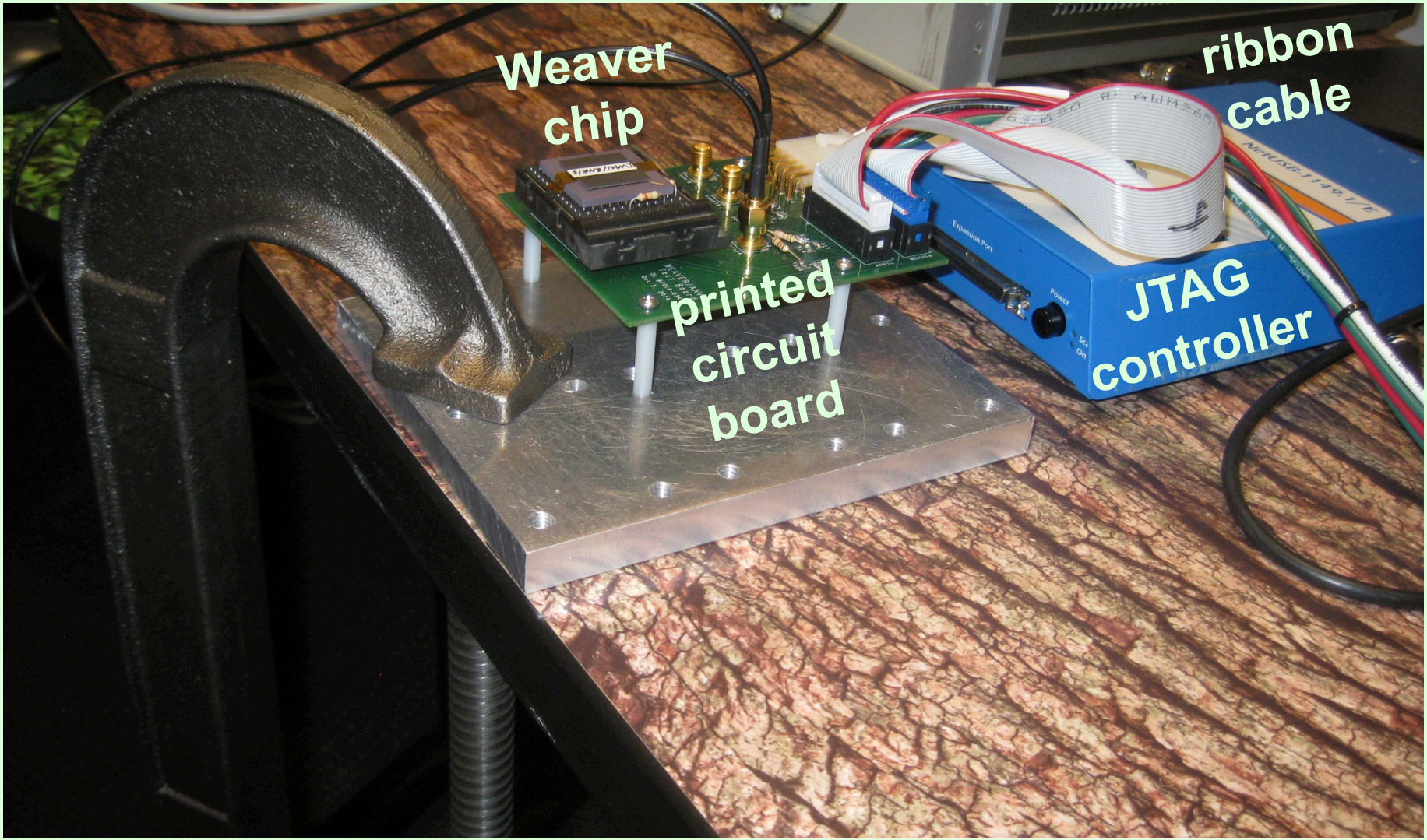
- An IEEE 5-wire test standard
- Test Access Port (TAP) has 5 pins
- Serial data ON and OFF chip
- Equipment available
- We have used for experiments
  - > Both synchronous and self-timed

- Widely used for commercial CMOS chips
- Unknown for superconducting chips

Weaver: CMOS self-timed 6 GHz

- Testable with 5 low-speed connections
  - > mega Hz signals to test giga Hz chip
- Test computer drives JTAG box
- JTAG box drives on-chip TAP controller
- TAP controller drives scan chains
- Scan-chains
  - > convert serial-to-parallel and parallel-to-serial
  - > and permit or forbid action

Weaver: CMOS self-timed 6 GHz

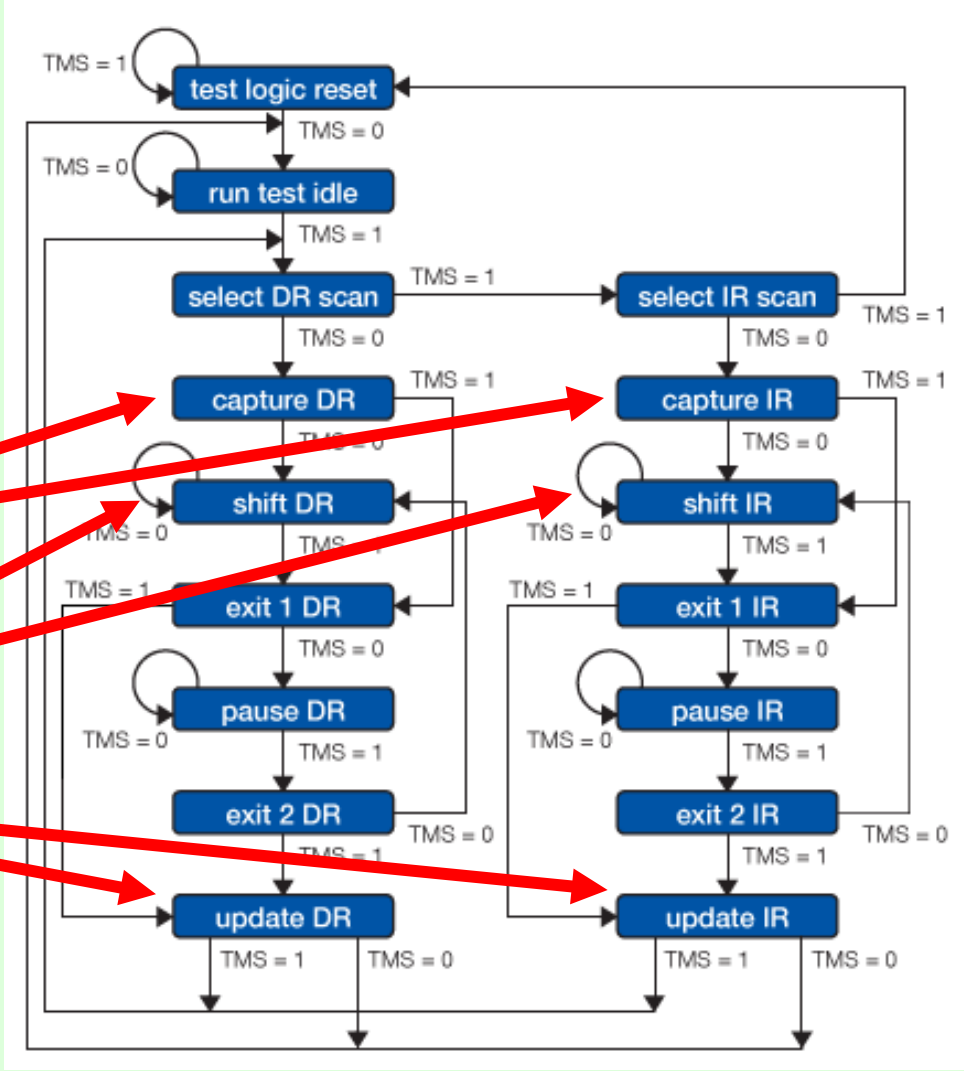


Testing Weaver

- Use JTAG to control
  - initial conditions
  - actions
    - permit action: chip runs
    - forbid action: chip stops
- Use JTAG to observe
  - final state
  - activity counters to calculate speed
- Test computer confirms data integrity
- Test computer plots throughput

TAP control state transition diagram

- Two shift registers
  - DR (data)
  - IR (instruction)
- TMS=0 actions
  - from CAPTURE
    ⇒ parallel read
  - from SHIFT
    ⇒ serial shift
  - from UPDATE
    ⇒ parallel write



Five low speed (mega Hz) wires

- Data in
- Data out
- Reset (optional)
- Clock (a **level** signal)
- TMS (a **level** signal)

CMOS levels

RSFQ pulses

- Use RSFQ **pulse** signals
  - tms0 ≅ (TMS = 0) & clock
  - tms1 ≅ (TMS = 1) & clock

RSFQ use 16 D2Latches, one-hot

- Only one latch is FULL (other 15 EMPTY)
- Each transition
  - **drains one latch**
  - and **fills another latch**

- IEEE standard permits counterflow clock
- Counterflow implies
  - **destination is drained** and guaranteed empty
  - **before the source emits a pulse**

Counterflow clocking sequence

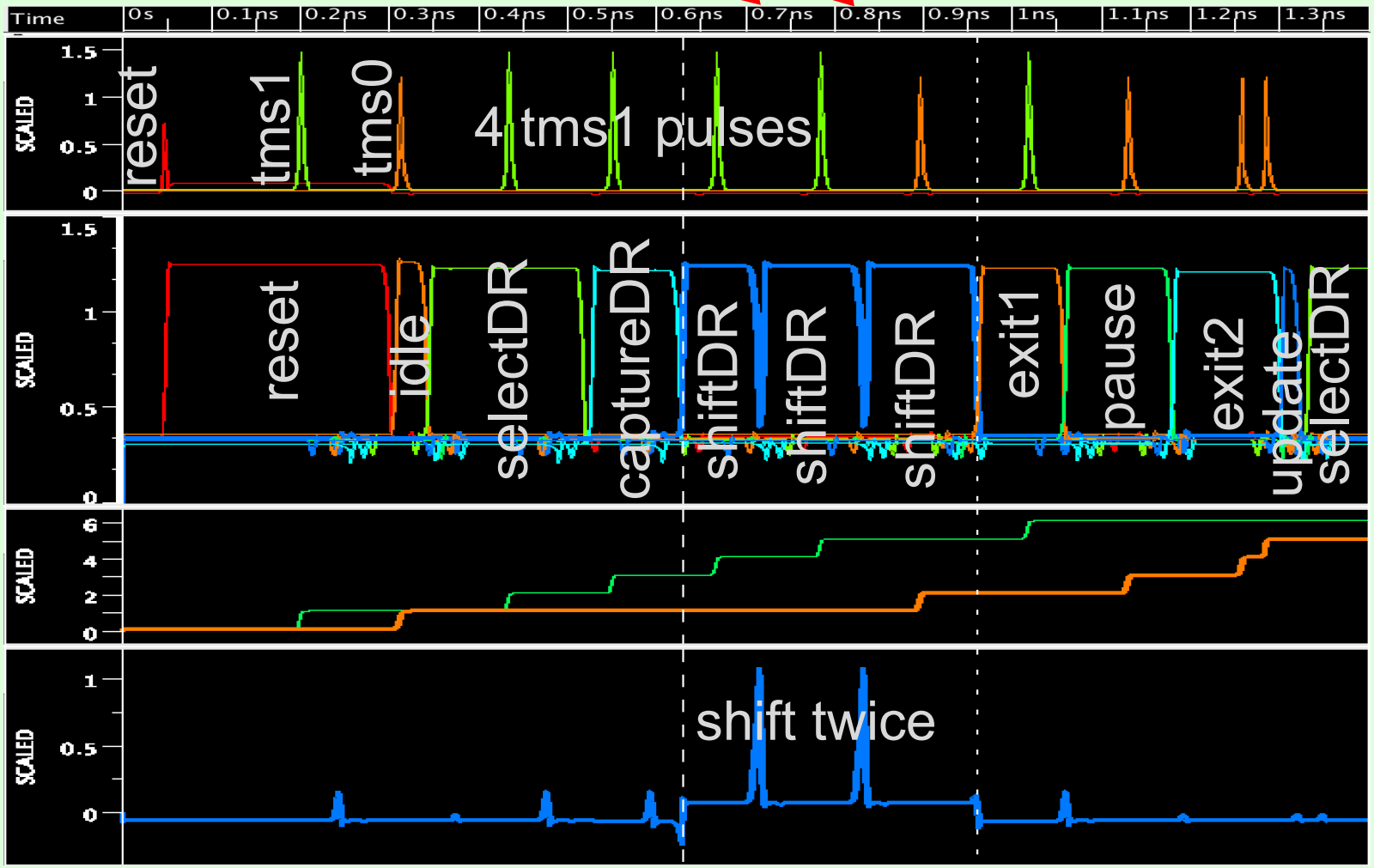
Sequence in which

- **tms0, tms1 pulses**
  - > reach state latches
- **state latches**
  - > 15 EMPTY are silent
  - > the one FULL latch emits a state transition pulse to successor
  - > successor already had its chance to act and so is EMPTY

Sequence for **tms0**	Sequence for **tms1**
run_test_idle	test_logic_reset
update_DR	select_IR_scan
pause_DR	select_DR_scan
exit_1_DR	run_test_idle
shift_DR	update_DR
exit_2_DR	exit_2_DR
capture_DR	pause_DR
select_DR_scan	exit_1_DR
test_logic_reset	shift_DR
update_IR	capture_DR
pause_IR	update_IR
exit_1_IR	exit_2_IR
shift_IR	pause_IR
exit_2_IR	exit_1_IR
capture_IR	shift_IR
select_IR_scan	capture_IR

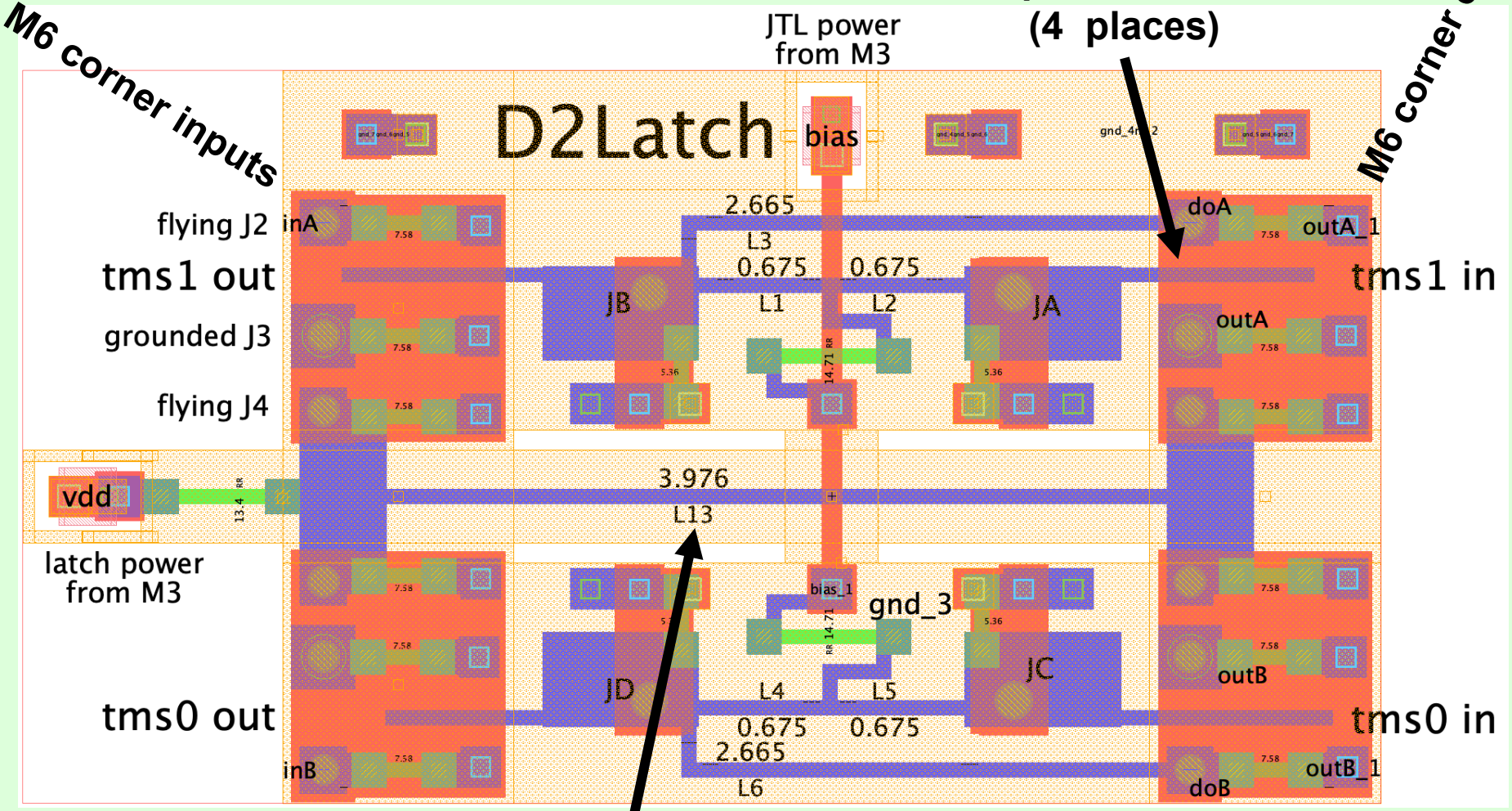
Simulation results

Four tms1 pulse actions:
go to state capture DR,
go to shiftDR, shift, shift

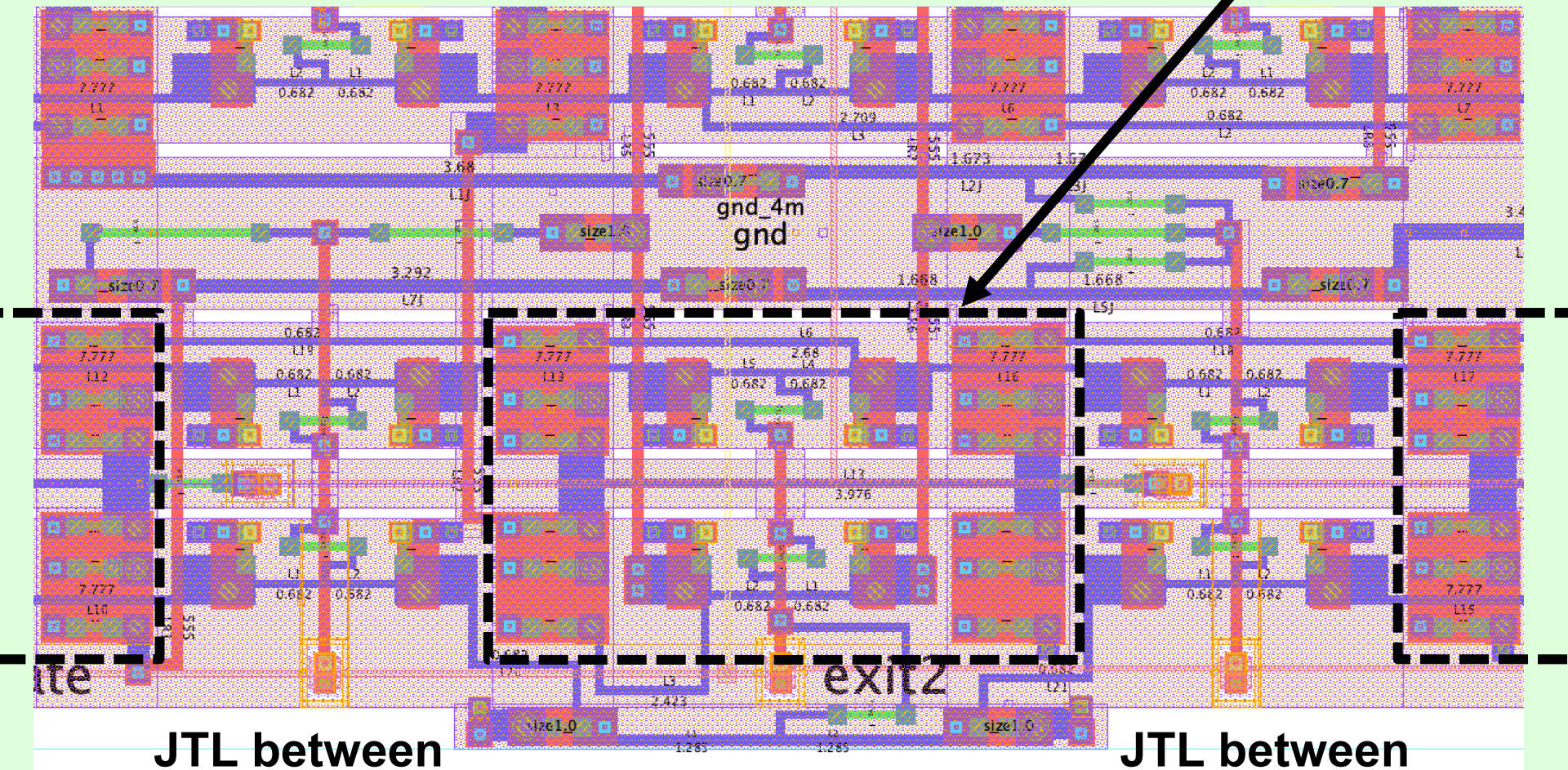


D2Latch layout with tms0, tms1

Lincoln Lab SFQ5ee process



TAP controller layout (near exit2)



JTL between two latches

tms JTL bypassing exit2

JTL between two latches

Our TAP controller

- Designed in Electric CAD system
  - > open-source
- Simulated in JoSIM and own VWsim (ACL2)
  - > equivalent results
- Patent free
  - > Lincoln Lab may distribute
  - > if support for test and revision is available

Our TAP controller

- Reduces test effort
- Permits remote testing

and

- Lets designers test their own chips
  - > Encouraging good test structures
  - > Increasing the number of chips tested per year

Discussion

D2Latch schematic

- 1 Lk = 125 10^{-6} Amp
- 1 oH = 2.632 10^{-12} Henry
- All JJs 0.707 Lk = 88 microAmp