INVITATION TO JOIN A NEW (UNDER)GRADUATE ECE COURSE:

SUPERCONDUCTING DIGITAL CIRCUITS

Term: Fall 2024 (30 Sep through 14 Dec 2024)
Time: Tuesdays and Thursdays from 06:40 PM to 08:30 PM
Where: EB Room 92 (by EB stairs on lower level of the Engineering Building (EB))
Schedule Type: Lecture
Course Delivery Method: In-Person Meeting (with Zoom link for remote attendance)
CRN:14613
Course Number: 410 and 510
Credit Hours: 4
Grade Mode: Graded Mode (A-F)
Contact: Christof Teuscher <teuscher@pdx.edu>, Ivan Sutherland ivans@cecs.pdx.edu
(see course Syllabus for the full list of contacts)

Abstract:
This course will teach the fundamentals of Superconducting Digital Circuits (SDC) technologies, review its history, explain why this 40 years old technology is currently used only in some military and intelligence niche applications, and review recent advances.

SDCs have the potential to consume 100 times less power (including cooling) while running 10 times faster than current CMOS based processors. This matters greatly! Contemporary data centers consume tens of Megawatts of power and struggle to meet the ever-rising demand on compute cycles from emerging AI applications. Power consumption and processing speed have become primary design objectives for large scale compute systems.

CMOS technology evolved over 3 decades and received untold billion in R&D investments. In contrast, SDC was largely abandoned. Thus, SDC is a relatively immature technology with great promises but also many challenges. There is a lot of room for innovation. Operating at speeds equivalent to several 100 GHz requires unconventional computing architectures and Computer Aided Design (CAD) tools, and has implication for nearly all layers of the hardware and software stack as we know it.

The area of Superconducting Digital Circuits is one of the rare branches of computer science and electrical engineering where you will find unclaimed low hanging fruit as well as intriguing research topics suitable for an MSc or a PhD thesis.

Instructors:
This course, endorsed by Prof. Christof Teuscher, has three guest experts: Ivan Sutherland, Andreas Nowatzyk, and Marly Roncken. Their bios follow on the next page.

Ivan Sutherland received his Ph.D. from MIT in 1963, and has held professorships at Harvard, the University of Utah, and Caltech. He joined Portland State University in 2009 as a Visiting Scientist to found the Asynchronous Research Center (ARC) with his research partner and wife, Marly Roncken. Sutherland holds the 1988 ACM Turing Award, the 2012 Kyoto Prize and over 70 US patents. He is a Fellow of the ACM and a Member of both the US National Academy of Engineering and National Academy of Sciences. Now 86 years of age, Ivan devotes full time to research, lectures, and writing.

Andreas Nowatzyk received MS equivalent degrees in Physics and Computer Science from the University of Hamburg, Germany and a PhD in Computer Science from Carnegie Mellon university with a dissertation on communication architectures for multiprocessor systems. After graduating from CMU in 1990, he joined Sun Microsystems, where he started a distributed shared memory multiprocessor project (S3.mp) that used a scalable, arbitrary topology switching fabric using serial, GB/s links to integrate all desktop-class system within one building into one computing platform that could share all resources. In 1996, he joined Digital's Western Research Lab that was subsequently acquired by Compaq and HP, where he used some S3.mp derived concepts and ideas for the Piranha microprocessor project. While Piranha is notable for being the first 8 core processor, it also included a high-speed interconnect system and the capability to scale to large numbers (> 1000) of processors without requiring any other components besides Piranha and memory ICs. In 2000, near the end of WRL, Andreas became an associate professor in the CMU ECE and Robotics departments where worked on reliability problems for large scale multiprocessor systems. He was the PI for the NSF and Intel funded TRUSS project that explored the idea of using cryptographic finger-prints on the evolution of the architectural state of processors in a large MP system to implement modular redundancy in a distributed fashion without significant increase of communication bandwidth requirements. In 2005, he moved to the Cedars Sinai Medical Center in LA where he works on real-time information (video and other data streams) processing systems for the future operating rooms. After his stint in the medical research community, he subsequently joined Microsoft, Google and finally VMware where he retired from their research groups when it was acquired by Broadcom. Besides working as a computer architect on MP systems, Andreas engaged in a large number of other hardware and software projects including computer chess (Deep Thought), 50+M pixel displays, Tb/s optical interconnect systems, wavelength agile lasers, avionics for the first RC plane to cross the Atlantic, and super-resolution microscopy.

Marly Roncken is a Research Professor with the Computer Science Department and Director and co-Founder of the Asynchronous Research Center (ARC) at Portland State University. Her focus is on modular design and test of (mostly) asynchronous circuits and systems for CMOS and superconducting technologies. As design aid, she and her students have developed a circuit-neutral Link-Joint model, which separates states in Links from actions in Joints, and which simplifies design integration, test, and debug. Prior to Portland State University, she worked at Intel Strategic CAD Labs and Philips Research. She has an MS (Drs) degree in Mathematics from the University of Utrecht, the Netherlands. For further information, see: https://arc.cecs.pdx.edu/.